IN THE DRAWINGS

The drawings of Figures 1, 6A and 6C have been amended. Clean drawing sheets including the amendments to Figures 1, 6A and 6C are attached hereto as Appendix I.

IN THE SPECIFICATION

Please amend the specification as follows below.

Please amend paragraph no. [0027] as follows:

"**[0027]** Fig. 1 illustrates an exemplary multi-port latch 100 in accordance with the prior art. The two port latch 100 has a data input "D0" (102) and a clock input "C0" (104) as its first port while a data input "D1" (106) and a clock input "C1" (108) feed the second port. If clock input "C0" is on, the latch 100 takes on the value of data input "D0" at its output L (110). Likewise, if clock input "C1" is on, the latch takes on the value of data input "D1" at the output L (110). If neither clock is on, the latch retains its previous value at the output L (110)."

Please amend paragraph no. [0035] as follows:

"**[0035]** Furthermore, the exemplary sequential circuit (400) and the sample clocking sequence are merely intended to be illustrative rather than restrictive. For example, a different circuit may be utilized with a different clocking sequence. Accordingly, it will be apparent to those with ordinary skill in the art that modifications may be made to the described embodiments, with the attainment of all or some of the advantages."

Please amend paragraph no. [0045] as follows:

"**[0045]** Fig. 6A illustrates an exemplary flow diagram of a method 600 for transforming a sequential logic design into combinational logic in accordance with an embodiment of the present invention. In one embodiment of the present invention, the method 600 takes as input a given [[,]] sequential logic design and a given clocking sequence. The method 600 then produces as output a combinational logic design that is logically equivalent to the original, sequential design under the influence of the given clocking sequence."

Please amend paragraph no. [0055] as follows:

"[0055] Fig. 6C illustrates an exemplary flow diagram of a method 680 invoked by the stage 616 of Fig. 6A in accordance with an embodiment of the present invention. The method 680 starts with a stage 682, which determines whether time T ~~precede~~ precedes the first time in which the primary inputs are forced. If so, a stage 684 produces B@T tied to an assumed, default value, for example, the same value as is assumed to be on this input at the start of a test (generally, high-Z for tester contacted, bi-directional pins, logicX for non-contacted pins, etc.). Thereafter, the method 680 terminates. If the stage 682 returns a "no," a stage 686 determines whether time T is a PI force. If so, a stage 688 produces B@T as a primary input and the method 680 terminates thereafter. Otherwise, a stage 690 produces B@T as a buffer (e.g., for tri-state or bi-directional inputs, a buffer capable of passing high-Z is used). The buffer may be connected to B@T-1. The method 680 continues by invoking the method 600 with block B and time T-1."

Please amend paragraph no. [0072] as follows:

"[0072] The foregoing description has been directed to specific embodiments. It will be apparent to those with ordinary skill in the art that modifications may be made to the described embodiments, with the attainment of all or some of the advantages. For example, the schemes, data structures, and methods described herein can also be extended to other applications. Also, [[Even]] even though AND/OR and tri-state implementations of the MUXes are discussed herein, it is envisioned that many other implementations are possible."